

CLAIMS

What is claimed is:

- 1 1. A method comprising:
2 detecting a plurality of subchannels comprising symbol-modulated
3 orthogonal subcarriers to generate a channelization vector indicating which of
4 the subchannels are active and which of the subchannels are inactive; and
5 performing data-symbol processing on the active subchannels in response
6 to the channelization vector to generate a bit stream from combined
7 contributions of the active subchannels.
- 1 2. The method of claim 1 further comprising generating a decoded bit
2 stream from combined contributions of the active subchannels.
- 1 3. The method of claim 1 wherein detecting comprises independently
2 detecting the subchannels of the plurality with a parallel set of matched filters.
- 1 4. The method of claim 1 wherein detecting comprises detecting the
2 subchannels with a parallel set of matched filters, wherein each of the matched
3 filters has a coefficient spectrum matched to a corresponding one of the
4 subchannels.
- 1 5. The method of claim 1 further comprising refraining from performing
2 data-symbol processing on the inactive of the subchannels in response to the
3 channelization vector.
- 1 6. The method of claim 1 further comprising providing the channelization
2 vector to data-symbol processing circuitry,
3 wherein the data-symbol processing circuitry is responsive to the
4 channelization vector to perform data-symbol processing on the active
5 subchannels, and

6 wherein the data-symbol processing circuitry is responsive to the
7 channelization vector to turn-off data-symbol processing on the inactive
8 subchannels.

1 7. The method of claim 6 wherein the performing data-symbol processing
2 comprises performing a fast-Fourier transform on only the active subchannels to
3 generate a bit stream from combined contributions of the active subchannels.

1 8. The method of claim 1 further comprising:
2 providing the channelization vector to combiner circuitry; and
3 combining, with the combiner circuitry, bit streams from the data-symbol
4 processing of the active subchannels to generate a combined bit stream.

1 9. The method of claim 8 further comprising refraining from combining a
2 processing output generated from the inactive subchannels.

1 10. The method of claim 1 further comprising:
2 generating a channelization vector for a plurality of received packets; and
3 repeating the detecting and performing the data-symbol processing for the
4 received packets, wherein the received packets comprise symbols modulated on
5 a plurality of orthogonal subcarriers of an orthogonal frequency-division
6 multiplexed signal.

1 11. The method of claim 1 further comprising receiving a synchronized
2 sequence of short-training symbols on at least two of the active subchannels, the
3 sequence of short-training symbols comprising at least a portion of preamble of a
4 received packet,
5 wherein the detecting comprises sampling the sequence of short-training
6 symbols on the at least two active subchannels, and
7 wherein the data-symbol processing comprises data-symbol processing a
8 sequence of long-training symbols and data symbols on the active subchannels,
9 the long-training symbols and data symbols following the sequence of short-
10 training symbols in the packet.

1 12. The method of claim 1 further comprising receiving synchronized
2 data streams on the active subchannels, the synchronized data streams being
3 preceded by a preamble, the channelization vector being generated from
4 detection of the preamble.

1 13. The method of claim 1 further comprising:
2 determining channel conditions of the subchannels, the channel
3 conditions including at least one of an interference level and fading; and
4 sending a request to a transmitter to refrain from transmitting on a
5 subchannel that has poor channel conditions.

1 14. An apparatus comprising:
2 short-training symbol processing circuitry to detect a training sequence
3 modulated on a plurality of subchannels and generate a channelization vector
4 indicating which of the subchannels are active and which of the subchannels are
5 inactive; and
6 data-symbol processing circuitry to process data symbols on the active
7 subchannels in response to the channelization vector.

1 15. The apparatus of claim 14 wherein the data-symbol processing
2 circuitry refrains from processing the inactive subchannels in response to the
3 channelization vector.

1 16. The apparatus of claim 14 wherein the short-training symbol
2 processing circuitry comprises a plurality of matched filters, each matched filter
3 having a coefficient spectrum matched to a corresponding one of the
4 subchannels.

1 17. The apparatus of claim 16 wherein the short-training symbol
2 processing circuitry further comprises:
3 non-coherent summaters to sum output from a corresponding one of the
4 matched filters;

5 threshold detectors to determine when the summed output from a
6 corresponding one of the summators exceeds a predetermined threshold; and
7 a multiplexer to combine outputs from the threshold detectors to generate
8 the channelization vector.

1 18. The apparatus of claim 14 wherein the data-symbol processing
2 circuitry comprises a combiner to generate a combined bit stream from
3 individual bit streams generated by data-symbol processing the active
4 subchannels in response to channelization vector, the combiner to refrain from
5 combining contributions from the inactive subchannels in response to the
6 channelization vector.

1 19. The apparatus of claim 14 wherein the data-symbol processing
2 circuitry comprises fast-Fourier transform (FFT) circuitry for a predetermined
3 number of the subchannels, channel equalization circuitry, demapping circuitry
4 and deinterleaving circuitry to perform data-symbol processing in parallel for the
5 predetermined number of the subchannels.

1 20. The apparatus of claim 19 wherein the data-symbol processing
2 circuitry further comprises:
3 a combiner to a combiner to generate a combined bit stream from
4 individual bit streams generated by data-symbol processing the active
5 subchannels in response to channelization vector; and
6 a decoder to decode the combined bit stream and generate a decoded bit
7 stream output.

1 21. The apparatus of claim 19 wherein the data-symbol processing
2 circuitry comprises four 64-bit fast-Fourier transform (FFT) processing circuits
3 to process four 20 MHz subchannels substantially in parallel.

1 22. The apparatus of claim 14 wherein the data-symbol processing
2 circuitry comprises wideband fast-Fourier transform (FFT) circuitry to
3 selectively perform an FFT on parallel groups of time-domain samples from the

4 active subchannels in response to the channelization vector and to selectively
5 refrain from performing the FFT on the parallel groups of time-domain samples
6 from the inactive subchannels in further response to the channelization vector.

1 23. The apparatus of claim 22 wherein the wideband fast-Fourier
2 transform (FFT) circuitry comprises a 256-bit FFT processing circuit to process
3 256 parallel symbols from a wideband channel comprised of up to four 20 MHz
4 subchannels.

1 24. The apparatus of claim 19 further comprising a wideband decoder to
2 generate a decoded bit stream from combined bit streams from the active
3 subchannels.

1 25. A receiver system comprising:
2 an omnidirectional antenna to receive symbol-modulated subcarriers over
3 a plurality of subchannels;
4 short-training symbol processing circuitry to detect the plurality of
5 subchannels and generate a channelization vector indicating which of the
6 subchannels are active and which of the subchannels are inactive; and
7 data-symbol processing circuitry to process data symbols on the active
8 subchannels in response to the channelization vector.

1 26. The system of claim 25 wherein the short-training symbol processing
2 circuitry comprises:
3 a plurality of matched filters, each matched filter having a coefficient
4 spectrum matched to a corresponding one of the subchannels;
5 non-coherent summators to sum output from a corresponding one of the
6 matched filters;
7 threshold detectors to determine when the summed output from a
8 corresponding one of the summators exceeds a predetermined threshold; and
9 a multiplexer to combine outputs from the threshold detectors to generate
10 the channelization vector.

1 27. The system of claim 25 wherein the data-symbol processing circuitry
2 comprises fast-Fourier transform (FFT) circuitry for a predetermined number of
3 the subchannels, channel equalization circuitry, demapping circuitry and
4 deinterleaving circuitry to perform data-symbol processing in parallel for the
5 predetermined number of the subchannels.

1 28. A machine-readable medium that provides instructions, which when
2 executed by one or more processors, cause said processors to perform operations
3 comprising:
4 detecting a plurality of subchannels to generate a channelization vector
5 indicating which of the subchannels are active and which of the subchannels are
6 inactive; and
7 performing data-symbol processing on the active of the subchannels in
8 response to the channelization vector.

1 29. The machine-readable medium of claim 28 wherein the instructions,
2 when further executed by one or more of said processors, cause said processors
3 to perform operations further comprise generating a decoded bit stream from
4 combined contributions of the active subchannels, and
5 wherein detecting comprises detecting the subchannels with instructions
6 that implement a parallel set of matched filters, wherein each of the matched
7 filters has a coefficient spectrum matched to a corresponding one of the
8 subchannels.

1 30. The machine-readable medium of claim 28 wherein the instructions,
2 when further executed by one or more of said processors, cause said processors
3 to perform operations further comprising performing a fast-Fourier transform to
4 generate a bit stream from combined contributions of the active subchannels.